CLAIMS

1. A semiconductor memory comprising:

a plurality of memory cells, arranged in a plurality of lines;

a plurality of memory cell access signal lines, each one associated with at least one respective line of memory cells, for accessing the memory cells of the at least one respective line of memory cells, each signal line having a capacitance intrinsically associated therewith,

characterised by further comprising:

a plurality of volatile memory cells, each volatile memory cell having a capacitive storage element,

each volatile memory cell being associated with a respective signal line, the capacitive storage element of each volatile memory cell comprising the capacitance intrinsically associated with the respective signal line.

2. The semiconductor memory according to claim 1, in which said capacitance is a parasitic capacitance intrinsically associated with the signal line.

3. The semiconductor memory according to claim 1 or 2, further comprising:

a signal line selector adapted to selecting the signal lines for accessing the memory cells, and

a volatile memory cell selector for selecting the volatile memory cells,

the volatile memory cell selector comprising the signal line selector.

4. The semiconductor memory according to claim 3, in which said lines of memory cells are bit lines of the memory.

5. The semiconductor memory according to claim 4, in which said signal lines are global bit lines and said bit lines are local bit lines of the memory, each global bit line being associated with at least two local bit lines, and comprising a local bit line selector for selectively connecting the local bit lines to the respective global bit line.

6. The semiconductor memory according to claim 5, in which said memory cells are arranged to form at least two memory sectors, the plurality of local bit lines associated with any global bit line comprising at least one local bit line in each of the at least two memory sectors.

7. The semiconductor memory according to claim 6, in which the local bit line selector keeps the local bit lines disconnected from the respective global bit line when accessing the volatile memory cells.

8. The semiconductor memory according to any one of the preceding claims, comprising a circuit for writing data into the volatile memory cells.

9. The semiconductor memory according to claim 8, in which the circuit for writing data into the volatile memory cells comprises a charging/discharging circuit for charging or discharging the capacitive storage elements, depending on the data to be written.

10. The semiconductor memory according to claim 8 or 9, comprising a circuit for sensing data stored in the volatile memory cells.

11. The semiconductor memory according to claim 10, in which the circuit for sensing data stored in the volatile memory cells comprises a circuit for rewriting the sensed data into the volatile memory cells.

12. The semiconductor memory according to claim 11, in which the circuit for rewriting data comprises the circuit for writing data.

13. The semiconductor memory of any one of the preceding claims, in which said memory cells are non-volatile memory cells.

14. A method of storing data, comprising:

providing a plurality of memory cells, arranged in a plurality of lines;

providing a plurality of semiconductor memory cell access signal lines (, each one associated with at least one respective line of memory cells, for accessing the memory cells of the at least one respective line of memory cells;

using the memory cells for storing first data;

characterised by further comprising:

using capacitances intrinsically associated with the memory cell access signal lines as capacitive storage elements, and

using the capacitive storage element for volatily storing second data.

15. A memory, comprising:

a plurality of bit lines;

a plurality of memory cells, each memory cell being selectively couplable to an associated bit line;

read-write circuitry coupled to the bit lines and operable in a first read mode to couple a selected memory cell to the associated bit line and to sense the bit line to detect the data stored in the selected memory cell and operable in a first write mode to couple a selected memory cell to the associated bit line and transfer data into the selected memory cell, and operable in a second read mode to select a bit line and isolate all memory cells from the selected bit line, and to sense the bit line to detect data stored on the selected bit line, and operable in a second write mode to select a bit line and isolate all memory cells from the selected bit line, and to transfer data into the selected bit line.

16. The memory of claim 15 wherein the memory cells comprise Flash memory cells and wherein memory cells including the selected bit lines comprise DRAM-like memory cells, with each bit line having an intrinsic capacitance that functions to store charge corresponding to data.

17. The memory of claim 15 wherein the memory cells are arranged in rows and columns and are grouped to form a first bank of memory cells and a second bank of memory cells.

18. The memory of claim 17 wherein the read-write circuitry is operable in the first read and write modes to access memory cells in the first bank and operable at the same time in the second read and write modes to access memory cells in the second bank, and vice versa.

19. The memory of claim 15 further comprising a plurality of main bit lines, the number of main bit lines being fewer than the number of bit lines, and wherein the read-write circuitry is further operable to selectively couple bit lines to the main bit lines during the first read and write modes and wherein the selected bit lines in the second read and write modes correspond to the main bit lines.

20. The memory of claim 15 wherein the read-write circuitry comprises:

row address decoders coupled through word lines to the memory cells;

column address decoders;

sensing amplifiers selectively couplable to the bit lines; and

write control circuitry selectively couplable to the bit lines.

21. A method of storing data in a memory-cell array, the memory-cell array including a plurality of memory cells and a plurality of bit lines, each memory cell being selectively couplable to an associated bit line, and the method comprising:

storing data in the memory cells in the array; and

storing data on the bit lines of the array.

22. The method of claim 21 further comprising:

selecting a memory cell in the array;

coupling the selected memory cell to the associated bit line;

reading data from or writing data to the selected memory cell over the bit line;

selecting a bit line;

isolating all memory cells from the selected bit line; and

reading data from or writing data onto the selected bit line.

23. The method of claim 21 wherein the memory-cell array comprises a first array and a second array, and wherein storing data in the memory cells comprises storing data in memory cells in one of the first and second arrays and wherein storing data on the bit lines of the arrays comprises storing data on the bit lines of the other one of the first and second arrays.

24. The method of claim 21 wherein storing data on the bit lines of the array comprises storing data on main bit lines of the array, each main bit line being couplable to a group of the plurality of the bit lines.

25. An electronic system, comprising:

a memory, including,

a plurality of bit lines;

a plurality of memory cells, each memory cell being selectively couplable to an associated bit line;

read-write circuitry coupled to the bit lines and operable in a first read mode to couple a selected memory cell to the associated bit line and to sense the bit line to detect the data stored in the selected memory cell and operable in a first write mode to couple a selected memory cell to the associated bit line and transfer data into the selected memory cell, and operable in a second read mode to select a bit line and isolate all memory cells from the selected bit line, and to sense the bit line to detect data stored on the selected bit line, and operable in a second write mode to select a bit line and isolate all memory cells from the selected bit line, and to transfer data into the selected bit line.

26. The electronic system of claim 25 wherein the electronic system comprises a computer system.

27. The electronic system of claim 25 wherein the memory cells comprise Flash memory cells.